28.10 104Gb/s 2^{11}-1 and 110Gb/s 2^{9}-1 PRBS Generator in InP HBT Technology

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PRBS generators are frequently used to produce data signals for testing high-speed components such as MUX and DEMUX circuits, as well as complete fiber-optic transmission links. Recent advances on high-speed ICs, e.g. a 165Gb/s 4:1 MUX [1], require PRBS signals at earlier unavailable data rates. Previous state-of-the-art results include a 100Gb/s 2^{7}-1 and a 72Gb/s 2^{31}-1 PRBS generator [2, 3]. Bit-rates exceeding 100Gb/s in combination with long bit sequences, as well as parallel outputs, are desired for testing 100Gb/s circuits and systems. In this paper, a 2^{11}-1 PRBS generator IC with one output providing data rates up to 104Gb/s and 4 parallel outputs up to 52Gb/s, is presented. The parallel outputs provide the required test signals for 4:1 MUXes with output bit rates up to 208Gb/s. In addition, a 2^{9}-1 PRBS generator with a single data output up to 110Gb/s is presented. The circuits are fabricated in an InP HBT technology with f_τ and f_{max} over 300GHz [4].

Simplified block diagrams of the 2^{11}-1 PRBS IC and its generator core are shown in Figs. 28.10.1 and 28.10.2. A parallel architecture, similar to [5], is employed for the generator core. It consists of 4 branches with an XOR gate and a shift register each, interconnected by multiple feedback paths. The OR gate allows insertion of logic ones into the generator core to bring it out of a potential all-zero state at start-up. The topology is derived from a linear feedback shift register with the generating polynomial $1+x^{9}+x^{11}$. Each of the core outputs q1 to q4 produces the same 2^{11}-1 bit sequence, but the signals are shifted apart by a quarter of the total sequence length (more precisely 512, 511, and 512 bits). They are connected via 50Ω drivers to the single-ended chip outputs Q1 to Q4. The high-speed differential output QF/QFB is obtained by multiplexing signals q2 and q4. In the auto-start circuitry, the signal q3 is low-pass filtered and compared with an internally set reference voltage to detect the absence of output data (which corresponds to an all-zero state of the core). If this is the case, a positive reset pulse is generated and applied to the core until the presence of data is detected. If needed, the reference voltage can be set externally through input REF. A pattern trigger output is provided for waveform viewing. The trigger is generated by feeding q3 to a ripple counter, consisting of 9 cascaded static dividers. This produces a squarewave signal with a period equal to that of a full 2^{11}-1 bit sequence [6]. The incoming clock signal is terminated in a 50Ω resistor at the input buffer where the single-ended-to-differential conversion takes place. The duty cycle of the differential clock can be adjusted by varying the bias voltage on input CREF. A static divider is included to provide a clock output at half the input frequency.

The 2^{9}-1 PRBS IC uses essentially the same architecture, but does not include any parallel low-speed outputs. The generator core implements the generating polynomial $1+x^{5}+x^{9}$ with only 2 parallel branches. This reduces the number of feedback paths, enabling a more compact and optimal layout of the core.

The challenges faced in the circuit design and layout involve synchronous clocking of the large number of FFs at clock frequencies exceeding 50GHz, minimizing propagation delays in feedback paths, and minimizing power dissipation, all of which can limit the ultimate performance of the chips. To minimize skew, the clock signal is distributed symmetrically from the center of the generator core, via separate buffers, to each branch of the core. All latches are implemented using CML (no emitter followers in the data path) for low current consumption. Figure 28.10.3 shows the schematic of a latch. The tail current is set by a resistor to reduce capacitive loading on the common emitter node and to enable a compact cell layout. The latch has open collector outputs and the load resistors of the preceding cell are placed at the input. High-enough bandwidth for latches and buffers is obtained by inductive peaking with microstrip lines. There is a trade-off between the amount of peak inductance that can be used and the layout size of the generator core, which affects the clock skew and the delays in the feedback paths. The XOR gates in the core, as well as the OR gate, are integrated in the master latch of each subsequent D-FF to reduce the gate delays (see Fig. 28.10.4). All interconnects between cells consist of microstrip transmission lines in metal layer 3 or 4 above a metal-2 ground plane. A double-stage driver is used for the high-speed data output to suppress clock feedthrough from the multiplexer output.

The fabricated chips are measured by wafer probing with V-connector probes and an Agilent sampling oscilloscope with precision time base and 70GHz remote sampling heads. Figure 28.10.5 shows the output eye diagrams and signal waveforms for the 2^{11}-1 PRBS generator at 100 and 104Gb/s. The upper traces show the high-speed output QF (single-ended) and the lower traces show one of the parallel outputs (Q2). When the clock frequency is increased above 52GHz, the output signals rapidly deteriorate and disappear.

The measured rms jitter on the high-speed output is typically below 400fs at an output rate of 80Gb/s and between 500 and 600fs at 100Gb/s. Figure 28.10.6 shows the measured results for the 2^{9}-1 PRBS generator. The jitter is noticeably larger at the maximum operation speed of 110Gb/s than at 100Gb/s (where it is typically $450fs_{rms}$). Both circuits operate continuously from 3Gb/s up to their maximum operation speed for a sine-wave clock signal. At maximum speed, the 2^{11}-1 and 2^{9}-1 PRBS generator ICs consume 2.8W and 2.2W, respectively, from a 3.5V supply. The single-ended output swing is $350mV_{pp}$. Micrographs of the ICs are shown in Fig. 28.10.7. Each chip occupies an area of 1.3 x 1.6mm^2.

Acknowledgements:
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References:

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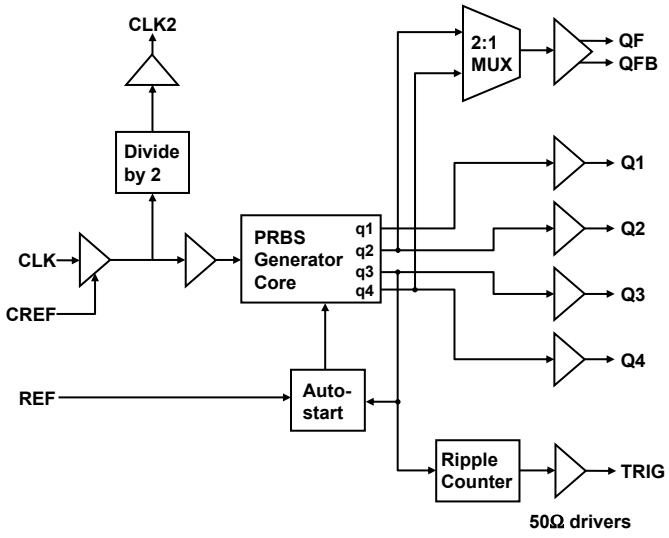

Figure 28.10.1: Block diagram of the 2^{11}-1 PRBS generator IC.

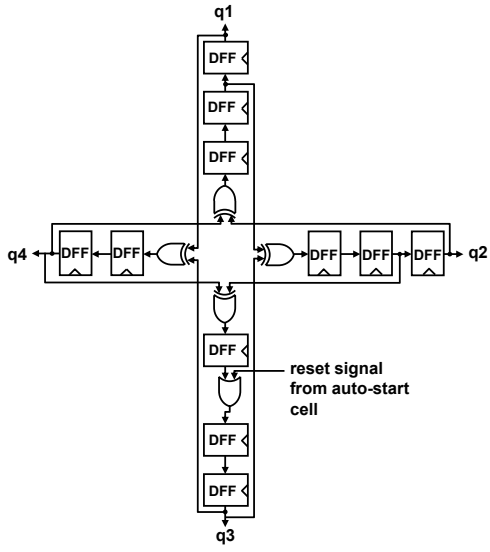

Figure 28.10.2: Block diagram of the 2^{11}-1 PRBS generator core.

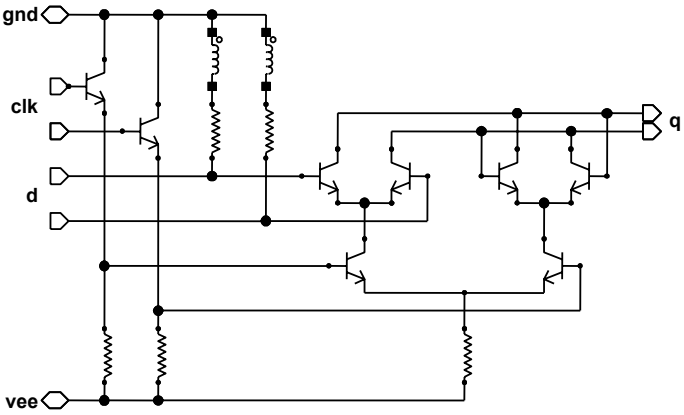

Figure 28.10.3: Schematic of latch.

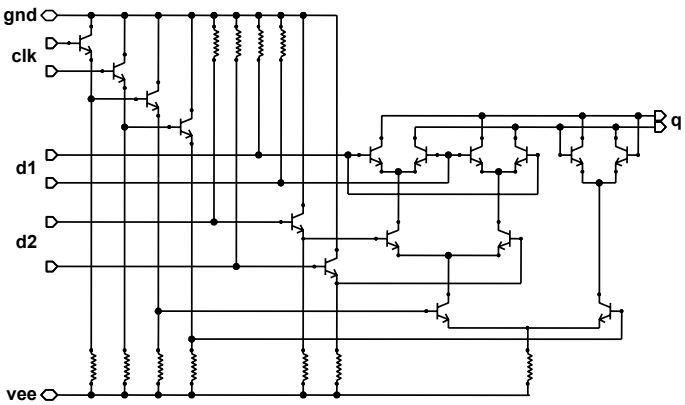

Figure 28.10.4: Schematic of latch with integrated XOR gate.

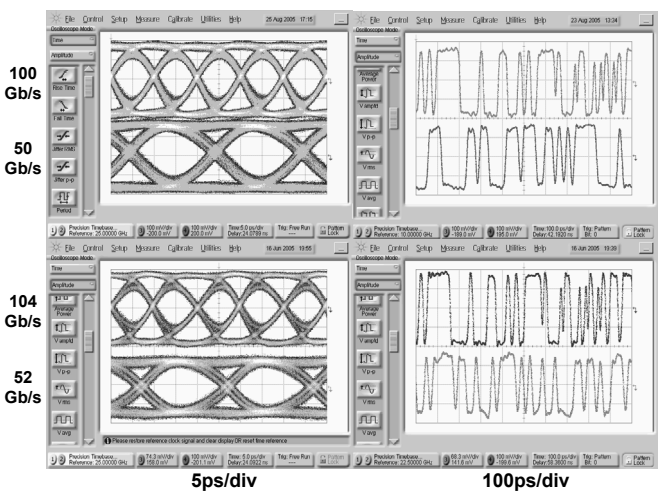

Figure 28.10.5: Eye diagrams and signal waveforms for 2^{11}-1 PRBS IC.

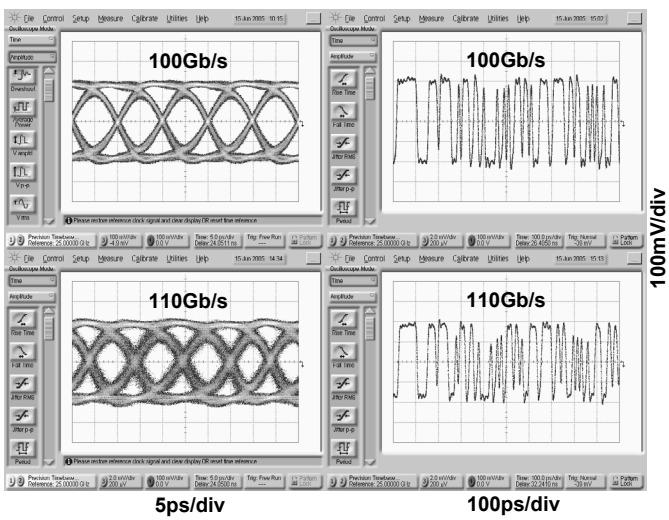

Figure 28.10.6: Eye diagrams and signal waveforms for 2^{9}-1 PRBS IC.

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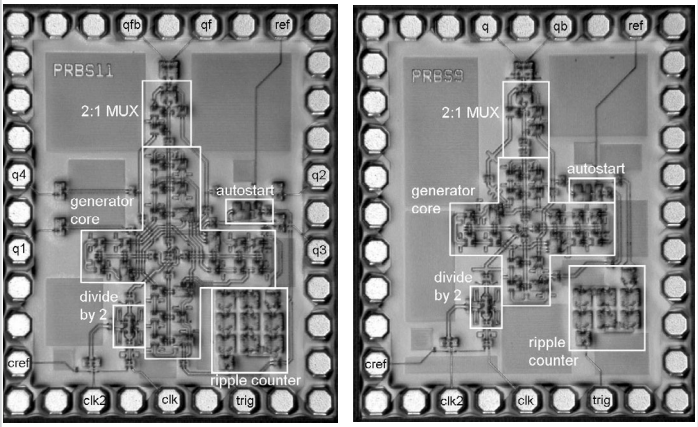

Figure 28.10.7: Micrographs of the 2^{11}-1 and 2^{9}-1 PRBS ICs.

